Project title: **TRECCINE**: Tool for the Rapid Evaluation, Comparison and Combination of INstruction-set Extension techniques

Project leader: Dr. Carlo Galuzzi **Function**: Assistant professor, DKE, Maastricht University, NL

Collaborators: Prof. Dr. Ralf Peeters and Dr. Matus Mihalak (Maastricht University, NL), Dr. Rene van Leuken (Delft University of Technology, NL) and Prof. Dr. Georgi Gaydadjiev (MAXELER, UK).

Proposal: In the last years, time-to-market and reduced development costs have become extremely important. For this reason, one emerging trend in computer design is component reuse or extension, for example by using reconfigurable devices (FPGAs), rather than designing and verifying a new product from scratch. The extension of the Instruction-Set Architecture (ISA) of a processor is one example of this trend. This allows to drastically increase the performance of execution of one or more applications on an architecture by implementing new instructions, optimized for the specific application(s). Many complex issues are involved in this customization process and knowledge in multiple fields of research (such as mathematics, engineering, etc.) is vital in order to tackle this problem. One of the main issues with the evaluation of existing techniques for Instruction-Set Extension (ISE) is the complete absence of a common tool and a methodology to compare them. Existing methods are usually limited to isolated issues involved in the process and their evaluation is based on sporadic comparisons on a limited number of benchmark applications, most of the time custom defined by the user. This makes it extremely hard, if not impossible, to perform objective evaluation and comparison of the different approaches.

The target of the proposed research is the development of novel methodologies for the extension of a given instruction set architectures customized either per application or per domain of applications and the development of a generic tool for the evaluation and comparison of (existing) ISE techniques for customizable/reconfigurable architectures. The tool, first and unique in its kind, will provide an effective instrument to test the qualities of different extension techniques on applications from different domains and it will allow the evaluation of techniques even when they are limited to only isolated issues involved in the customization process

Requirements candidate: A highly motivated student with good English communication skills, proactive and resolute attitude and with, preferably, a master degree in (applied) mathematics or (computer) engineering. Knowledge on the following subjects is considered an asset: Graph Theory, Statistics, Matlab, Algorithms (Exact and Approximation), Field-Programmable Gate-Array (FPGA), programming in C++, System C, and Python, and Compilers (optimization).

Keywords: Instruction Set Architecture Extension, Reconfigurable Computer Architecture, FPGA, Graph Theory.

Selected publications:

1. A. Pulli, C. Galuzzi, and G. Gaydadjiev: Towards Domain-Specific Instruction-Set Generation, in: 2014 International Conference on Field Programmable Logic and Applications (FPL 2014), Munich, Germany, September 2014
2. C. Galuzzi and K. Bertels: The Instruction-Set Extension Problem: A Survey, in: ACM Transactions on Reconfigurable Technology and Systems (TRETS), Volume 4, Issue 2, June 2011, pp. 18:1–18:28, DOI: 10.1145/1968502.1968509.
3. Paolo Ienne Rainer Leupers: Customizable Embedded Processors, Morgan Kaufmann, 2006
4. Carlo Galuzzi, Automatically Fused Instructions - Algorithm for the Customization of the Instruction-Set of a Reconfigurable Architecture , PhD Thesis, TU Delft, May 2009
5. C. Galuzzi, E. Moscu Painante, Y. D. Yankova, K. Bertels and S. Vassiliadis, Automatic Selection of Application-Specific Instruction-Set Extensions, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 160-165, Seoul (Korea), October 2006.